AMENDMENTS TO THE SPECIFICATION

Page 2, please replace paragraph [0005] with the following new paragraph:

[0005] FIG. 1 is a plan view illustrating the exterior of a semiconductor integrated circuit device 100 having a general structure of pads with a center layout. Referring to FIG. 1, bonding pads PD1,PD2~PDn are disposed in one row between memory cell array regions 10, 20. A place where the bonding pads PD1,PD2~PDn are located becomes an upper part of a peripheral circuit region 30. Such a layout of the bonding pads is called a pads center layout system. Wire bonding for pads with the pads center layout structure may be performed over upper parts of the memory cell array region 10 and the memory cell array region 20 on chip 100. In other words, part of the leads from a lead frame may be disposed close to the memory cell array region 10, and the remaining leads may be disposed close to the memory cell array region 20. Wires connecting between each of the leads and each of the pads may be formed over an upper part of the memory cell array regions 10, 20 thus undergo a bonding operation. The pads center layout structure has a shortcoming in that cell array regions are separated from each other because the pads PD1~PDn are disposed between the memory cell array regions 10, 20, and this detrimentally influences signal integrity.

Page 3, please replace paragraph [0006] with the following new paragraph:

[0006] FIGS. 2a and 2b are plan views showing the exterior of a semiconductor integrated circuit device having a general structure of an edge pad layout system. FIG. 2a illustrates a layout of bonding pads PD1~PDn, PDa1~PDan disposed in parallel only on two sides of the chip ~~10~~100. While, FIG. 2b illustrates a layout of bonding pads disposed on all four sides of the chip 100. In wire bonding pads of an edge pad layout system, there may be no wire formed over an upper part of a memory cell array region 11, but a reduction of the chip size may be difficult to realize because the pads are disposed on several sides of the chip 100. Also, signal integrity may be reduced by the dispersed layout of the bonding pads.